Code :RR320405 **RR**

III B.Tech II Semester(RR) Supplementary Examinations, April/May 2011
VLSI DESIGN
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE questions
All questions carry equal marks
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1. (a) With neat sketches explain the Drain characteristics of the p-channel Enhancement MOSFET.
   (b) An p-MOS Transistor is operated in the Active region with the following parameters $V_{GS} = -4.5V$; $V_{tp} = -1V$; $W/L = 95$; $\mu nCox = 95\ \mu A/V^2$
   Find its drain current and drain source resistance.
2. With neat sketches explain how pnp transistor is fabricated in Bipolar process.
3. Design a stick diagram for n-MOS Ex-OR gate.
4. Design a layout diagram for the NMOS logic shown below $Y = \overline{(A + B + C)}$
5. Calculate on resistance of the circuit shown in Figure 1 from V_{DD} to GND. If n-channel sheet resistance Rsn = 10^4 Ω per square and p-channel sheet resistance $Rsp = 3.5 \times 10^4 \Omega$ per square. [16]

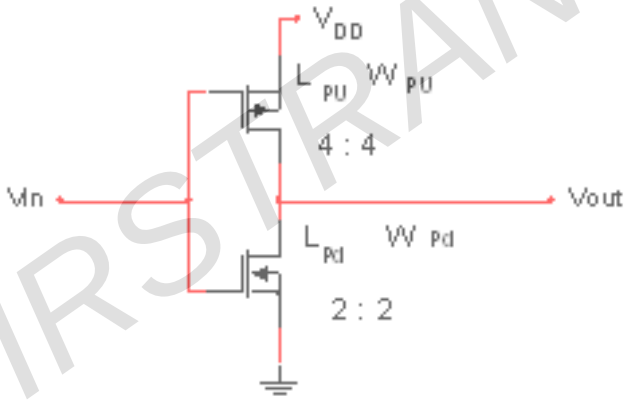

Figure 1:

6. Implement 4:1 Multiplexer using PLA.
7. What is need for RTL simulation? Clearly explain RTL simulation flow in the ASIC design flow and also mention few leading simulation tools.
8. With neat sketches explain the oxidation process in the IC fabrication process.

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